We claim:

1. A method for planarizing an MRAM cell structure on an MRAM chip having an insulation layer with an uneven top surface formed on an MTJ which is comprised of a bottom layer on a substrate, a free layer on the bottom layer, and a cap layer on the free layer, comprising:

(a) performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer; and

(b) performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized at a certain thickness below said cap layer.

2. The method of claim **1** wherein the insulation layer is comprised of silicon oxide or a low k dielectric material and has a thickness of about 800 to 2000 Angstroms above said cap layer before said CMP step.

3. The method of claim **1** wherein said certain thickness above the cap layer is about 60 to 200 Angstroms.

4. The method of claim **1** wherein said certain thickness below the cap layer is about 50 to 190 Angstroms.

5. The method of claim **1** wherein the cap layer is comprised of Cu, Ru, or a composite layer with an upper Ru layer.

6. The method of claim **5** wherein the cap layer has a thickness that is reduced by less than 5 Angstroms during said etch back step.

7. The method of claim **1** wherein etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer.

8. The method of claim **1** wherein the etch back step is comprised of an overetch portion.

9. The method of claim **1** wherein said MRAM chip is further comprised of a plurality of MTJs that have a cap layer thickness variation of less than +/- 5 Angstroms after the etch back step.

10. The method of claim **9** wherein the cap layer thickness is between about 50 and 400 Angstroms.

11. A method for fabricating an MRAM cell structure on an MRAM chip, comprising:

(a) forming a first conductive layer comprised of a first line on a substrate;

(b) forming an MTJ on said first line, said MTJ has a bottom layer, a free layer on said bottom layer, and a cap layer on said free layer;

(c) depositing an insulation layer on said MTJ and on said substrate;

(d) performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer;

(e) performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized at a certain thickness below said cap layer; and

(f) forming a second conductive layer on said insulation layer and cap layer, said second conductive layer is comprised of a second line that contacts the top surface of said cap layer.

12. The method of claim **11** wherein the bottom layer of said MTJ is a composite layer comprised of a seed layer on said first line, an AFM layer on the seed layer, a pinned layer on the AFM layer, and a tunnel barrier layer on the pinned layer.

13. The method of claim **11** wherein the first line is comprised of copper and is a bottom electrode, a bit line, or a word line.

14. The method of claim **11** wherein the second line is comprised of copper and is a word line or bit line.

15. The method of claim **11** wherein said certain thickness above the cap layer is about 60 to 200 Angstroms.

16. The method of claim **11** wherein said certain thickness below the cap layer is about 50 to 190 Angstroms.

17. The method of claim **11** wherein the cap layer has a thickness between about 50 and 400 Angstroms and is comprised of Cu, Ru, or a composite layer with an upper Ru layer.

18. The method of claim **17** wherein said cap layer has a thickness that is reduced by less than 5 Angstroms during said etch back step.

19. The method of claim **11** wherein the MTJ has a width from about 0.2 to 0.9 microns.

20. The method of claim **11** wherein the insulation layer is comprised of silicon oxide or a low k dielectric material and has a thickness of about 800 to 2000 Angstroms above said cap layer before said CMP step.

21. The method of claim **11** wherein etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer.

22. The method of claim **11** wherein the etch back step is comprised of an overetch portion.

23. The method of claim **11** wherein said MRAM chip is further comprised of a plurality of MRAM cells that have a distance variation of less than +/- 5 Angstroms from a free layer to an overlying second line after the etch back step.

24. The method of claim **11** wherein the MRAM chip is further comprised of an array of lines in said first conductive layer that are parallel to said first line, an array of lines in the second conductive layer that are parallel to the second line, and an array of MTJs formed at each location where a second line crosses over a first line wherein the distance between a free layer and an overlying second line is maintained to within 10 Angstroms.

25. An MRAM cell structure formed on a substrate, comprising:

(a) a first conductive layer formed within a first insulation layer on said substrate, said first conductive layer is comprised of an array of parallel first lines having a first width that are coplanar with said first insulation layer;

(b) an array of MTJs formed on said parallel first lines, said MTJs have a length and width and are comprised of a bottom layer, a free layer on the bottom layer, and a cap layer on the free layer wherein the cap layer has a thickness and a top surface;

(c) a second insulation layer formed on said first insulation layer and on said first conductive layer, said second insulation layer is adjacent to said MTJs and has a planar top surface which is a certain distance below the top surface of said cap layer; and

(d) a second conductive layer comprised of an array of parallel second lines having a second width that are aligned in a direction perpendicular to said first lines and

wherein the array of second lines is formed over the MTJs so that an MTJ is located at each location where a second line crosses over a first line.

26. The MRAM cell structure of claim **25** wherein the first lines and second lines are comprised of copper, the first lines are bit lines, and the second lines are word lines.

27. The MRAM cell structure of claim **25** wherein the first lines and second lines are comprised of copper, the first lines are word lines, and the second lines are bit lines.

28. The MRAM cell structure of claim **25** wherein said cap layer is comprised of Cu, Ru, or a composite layer with an upper Ru layer.

29. The MRAM cell structure of claim **25** wherein said cap layer has a thickness of about 50 to 400 Angstroms.

30. The MRAM cell structure of claim **25** wherein said second insulation layer is comprised of silicon oxide or a low k dielectric material and said certain distance below the top surface of said cap layer is about 50 to 190 Angstroms.

31. The MRAM cell structure of claim **25** wherein the distance from a free layer to an overlying second line has a variation of less than +/- 5 Angstroms.

32. The MRAM cell structure of claim **25** wherein the bottom layer is comprised of a seed layer formed on a first line, an AFM layer on said seed layer, a pinned layer on said AFM layer, and a tunnel barrier layer on said pinned layer.

33. The MRAM cell structure of claim **25** wherein the width of said MTJ is less than or equal to said first width and the length of said MTJ is less than or equal to said second width.

34. The MRAM cell structure of claim **25** wherein the width of said MTJ is from about 0.2 to 0.9 microns.